WE CLAIM:

Sub a3

1. A method for clocking video data to reduce beat patterns, comprising:

receiving a video data signal having a predetermined pixel frequency, the video data signal being provided by video data signal circuitry;

providing a local clock signal to re-clock the video data signal between the video data signal circuitry and output circuitry, thereby removing interfering influence of other clock signals on the predetermined pixel frequency.

2. The method of claim 1, wherein the video data signal is received within an integrated video display system.

3. The method of claim 1, wherein the video data signal is generated within an integrated video display system.

4. The method of claim 1, wherein the output circuitry comprises a digital-to-analog converter subcircuit.

5. The method of claim 4, wherein providing the local clock signal comprises latching the video data signal with at least one latching subcircuit clocked by the local clock signal.

6. The method of claim 5, wherein the latching subcircuit comprises at least one flip-flop configured to latch the video data signal through to the output circuitry, the flip-flop being clocked by the local clock signal.

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7. An integrated video display system for providing a video signal having reduced beat patterns, comprising:

a video data circuit coupled to an output circuit through a latching circuit, the video data circuit being configured to provide a video data signal based on a pixel frequency; and

a re-clocking circuit coupled to the latching circuit, the re-clocking circuit being configured to provide a local clock signal for re-clocking the video data signal through the latching circuit,

wherein the video data signal is provided to the output circuit based on the local clock signal.

8. The integrated video display system of claim 7, wherein the pixel frequency is based on an external clock reference and wherein the re-clocking circuit is based on the external clock reference.

9. The integrated video display system of claim 7, wherein the latching circuit comprises at least one flip-flop configured to latch the video data signal through to the output circuit, the flip-flop being clocked by the local clock signal.

10. The integrated video display system of claim 9, wherein the flip-flop is part of a final stage for the video data signal prior to being coupled to the output circuit.

11. The integrated video display system of claim 7, wherein the output circuit comprises a digital-to-analog converter subcircuit.

12. The integrated video display system of claim 7, further comprising a selection circuit for selectively switching between conventionally clocking the video data signal based on the pixel frequency and re-clocking the video data signal based on the local clock signal.

13. An integrated video display system for providing a video signal having reduced beat patterns, comprising:

a video data source based on a predetermined pixel frequency;

an output circuit;

a conventional clocking circuit including a clock signal based on the predetermined pixel frequency;

a re-clocking circuit having a frequency based on a clock signal provided by a local clock generator; and

a select switch for selectively coupling the video data source to the output circuit based on either the conventional clocking circuit or the re-clocking circuit,

wherein interfering influence of other clock signals on the predetermined pixel frequency is removed if the re-clocking circuit is coupled between the video data source and the output circuit.

14. The integrated video display system of claim 13, wherein the predetermined pixel frequency is based on an external clock reference and wherein the local clock generator is based on the external clock reference.

15. The integrated video display system of claim 14, wherein the local clock generator provides a pixel clock signal to the video data source on which to base the predetermined pixel frequency.

16. The integrated video display system of claim 13, wherein the output circuit comprises a digital-to-analog converter subcircuit.

17. The integrated video display system of claim 13, wherein the re-clocking circuit comprises at least one latching subcircuit clocked by the local clock generator.

18. The integrated video display system of claim 17, wherein the latching subcircuit comprises at least one flip-flop configured to latch the video data source through to the output circuitry, the flip-flop being clocked by the local clock signal.

19. The integrated video display system of claim 18, wherein the latching subcircuit is coupled to the video data source and the output circuitry, and wherein the output circuitry comprises a digital-to-analog converter subcircuit.

20. The integrated video display system of claim 19, wherein the latching subcircuit is the final stage of a video data path between the video data source and the output circuitry.